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EXAMINER

THOMAS, SHANE M

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

DETAILED ACTION

This Office action is responsive to the amendment filed 5/5/2008. Claim 12 is currently pending. Applicants' arguments and amendment to the claims have been carefully and considered, but they are not persuasive and do not place the claims in condition for allowance. Accordingly, this action has been made FINAL.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beletsky et al (U.S. Patent Application Publication No. 2004/0148153) in view of Chen (U.S. Patent Application Publication No. 2002/0156990).

As per claim 12 and 8, Beletsky teaches **a method for rearranging data comprising the steps of:**

a) storing a plurality of data (shadow read data) **in a first data storage section** (first column portion of circular buffer 40 - figure 6) - ¶65 teaches reading data from the address via a read port of a RAM (¶13) and storing the read out data in circular buffer;

b) storing data rearrangement information (the address associated with each data entry of circular buffer 40 - figure 6) **in a stack** (as circular buffer 40, itself, may be considered a

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LIFO buffer, ¶65, it can therefore be seen that the data portion column is operated as a stack since stacks operate on the same “last-in, first-out” functionality);

c) reading the data stored in the first data storage section (during a rewind period, ¶62, data is read out from the circular buffer first column portion) , **and storing the data in a rearranged order** (data is considered to be stored in the RAM in a “rearranged order” when taken in reference with the order of the data when stored in the circular buffer 40) **in a second data storage section** (system RAM via RAM’s write port 20, figure 1) **based on the data rearrangement information stored in the stack** (address data from second column portion of the circular buffer 40 - figure 6 - is used to store the corresponding data to a specific address back in RAM - ¶63) In other words, during random writes to the RAM, data that is to be overwritten is stored in the circular buffer 40 in order to be rewound at a later point. This data is stored in a last-in, first-out order within circular buffer 40 as discussed. When data is rewound, and therefore stored back in the RAM, the data will be written back to its original location in the order the system originally over-wrote the data. Therefore, since the data is stored in the circular buffer in the order by which it is overwritten during writes to the RAM, and since data can be stored in any order in RAM, according to the program write instructions that are being executed by the system, it can therefore be seen that the data stored in the circular buffer will be stored back in the RAM in a different order that it was stored in the circular buffer 40.

d) addressing the data stored in the second data storage section by the data rearrangement information (data may be addressed in the second storage section via the data in the rearrangement information as the rearrangement information, itself, is the corresponding address of each data element that is rewritten into RAM during the rewind periods - ¶62).

Beletsky further teaches **wherein the reading and the storing are carried out by using an address conversion table** (the Examiner is considering the collection of data rearrangement entries corresponding to a single rewind interval (see figure 7) to be an address conversion table as it would comprise the collection of address of the system RAM that have had their corresponding data entries converted or overwritten with new data) **and a corresponding stack pointer** (the state machine 45 - figure 1 - controls a stack pointer as taught in ¶61, that is used during the reading of data from the stack 40 into the RAM).

Beletsky teaches the use of a stack pointer (the state machine 45 - figure 1 - controls a stack pointer as taught in ¶61, that is used during the reading of data from the stack 40 into the RAM) but does not specifically state that the stack pointer is stored in a **register**. By storing the current stack pointer in a register, the system of Beletsky would have been able to maintain the value of the stack pointer while performing a current operation, as it is well known in the art to store values in a register in order to utilize the values. Chen teaches such operation in paragraphs ¶6, ¶7, and ¶12. Chen discusses a current address register for use in a circular buffer. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the rearrangement scheme of Beletsky with the teaching of using a register to store the current address of Chen in order to have produced the predictable result of knowing which address was currently being operated on in the system of Beletsky.

Response to Arguments

Applicant states on page 3 of the Arguments/Response filed 1/29/2008 that "[t]he Examiner indicated that claim 13 is objected to as depending from rejected base claims, but indicated that this claim would be allowable if rewritten in independent form to include the limitations of the base claim and any intervening claims." Such an amendment has not been made to presently pending claim 11. Applicant has broadened original claim 13 to state that "the reading and storing are carried out using ... a register." While this is similar to original claim 13, such an amendment in light of the interviews conducted on 1/11/08 and 1/15/08. The Examiner made it clear in those interviews and the accompanying Interview Summaries that while an indefinite issue should have been identified in an earlier Office action with respect to claim 13, the potential allowable subject matter within the claim, when read in light of the specification, was that in certain instances, Applicant invention substituted a register for the stack pointer. The Examiner suggest in the Interview Summary filed 1/16/2008 to "amend claim 1 to include the limitation of claim 13 and intervening claim 11 and also, using language from the specification, indicate how the stack pointer is used during certain instances and during other instances the value contained in a register is substituted for that stack point."

The Examiner reiterated this point in the subsequent Interview Summary filed 1/17/2008 by stating "claim language emphasizing ... that, at least during some circumstances, a value in a register is used (e.g. "substituted") instead of the stack pointer" and that if that subject matter is properly incorporated, it would overcome the prior art-based rejections.

Applicant elected to amend claim 11 to merely state that a "register" is used with the "reading and storing." As such, the Examiner has cited the prior art reference of Chen to teach

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that a current address register may be used to hold the value of the current address of a circular buffer when operating on that buffer address.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chou (U.S. Patent Application Publication No. 2003/0033499) teaches the use of a current address register with a circular buffer (¶¶43-44).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHANE M. THOMAS whose telephone number is (571)272-4188. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shane M. Thomas/
Patent Examiner

4 August 2008